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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHACE, CHRISTIAN	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,960	WILCOX ET AL.	
	Examiner	Art Unit	
	Christian P. Chace	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/26/04, 7/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 28 May 2004 has been entered.

Response to Amendment

The Office action has been issued in response to amendment filed 28 may 2004, as discussed supra. Claims 1-42 are pending. Applicants' arguments have been carefully and respectfully considered, and they are not persuasive. This action is NOT final, as it is a first action following an RCE.

Drawings

Drawing corrections submitted 28 May 2004 have been approved by examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6, 15-17, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al (US Patent #6,058,059).

The claims as broadly construed and interpreted, particularly with regard to the memory "bus," "read on" a method and apparatus disclosed by Huang et al, and thus the invention as broadly set forth in the claims is seen to be anticipated by Huang et al. (In this regard, also see MPEP 706.02(m) regarding form paragraph 7.27.)

With respect to claim 1, as well as claim 15, Huang et al discloses a method and apparatus for controlling amplification in a memory of a computer system so as to reduce power consumption. Huang et al discloses providing amplifiers for amplifying data signals from a memory bus (Huang et al teaches that data signals on complementary pairs of bit lines, which represent bits of data output from an SDRAM, may be amplified by sense amplifiers. (See column 3, lines 13-27, and Figure 1, e.g., and providing a "first circuit" for "sampling" the amplified data signals (the amplified data signals may be "sampled" by a pair of latch circuits 22, 32 and an output buffer 24, e.g.).

Huang et al further teaches providing ("second") circuitry for selectively disabling the amplification in response to the absence of a predetermined operation occurring over the memory bus (Huang et al teaches selectively disabling the sense amplifiers when a predetermined operation such as a read operation is complete, i.e. "in the absence of" a predetermined operation such as a read operation. See column 1, lines 46-51', column 2, lines 39-54., column 5, line 48 to column 6, line 24, e.g.).

With respect to claims 2-3 and 6, as well as claims 16-17, Huang et al teaches that the "selectively disabling" comprises selectively disabling sense amplifiers, and that the selectively disabling is performed in response to the end or completion of a particular predetermined operation such as a read data output operation (again see column 1, lines 46-51, and column 6, lines 17-24).

With respect to claim 19, the apparatus of Huang et al includes circuitry for controlling various components of a memory and thus the "apparatus" of Huang et al may be broadly considered to be a memory "controller."

With respect to claim 20, Huang et al teaches that the apparatus may comprise a memory device such as an SDRAM device.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Taruishi et al (U.S. Patent 6,339,552).

The claims "read on" a method and apparatus disclosed by Taruishi et al, and thus the invention as broadly set forth in the claims is seen to be anticipated by Taruishi et al.

More specifically, with respect to claims 1 and 8, as well as claims 15 and 21, 27, 29, and 31-42, Taruishi et al (U.S. 6,339,552) disclose a method and apparatus for controlling amplification in a memory of a computer system so as to reduce power consumption, as in the claimed invention. Taruishi et al discloses providing amplifiers for amplifying data signals from a memory bus. (Taruishi et al disclose that sense amplifiers within data 1/0 circuits (DIO0-DIO3) in Figure 1 are used to amplify data signals from a memory "bus" in a well known manner. See column 5, lines 59-64, e.g.) and providing a "first circuit" for "sampling" the amplified data signals (a data output circuit 4 in Figure 1 may be used to "sample" the amplified data signals, e.g.). Taruishi et al further teaches providing ("second") circuitry for selectively enabling and disabling the amplification in response to whether a predetermined operation occurs over a memory bus. Taruishi et al teaches selectively enabling the sense amplifiers in response to a "predetermined" operation occurring over a memory bus in a particular bank and selectively disabling the sense amplifiers when a predetermined operation is not occurring over a memory bus in a particular bank. See column 6, lines 33-40, e.g.). Attention is also respectfully directed to column 2, lines 24-41 and 57-62., column 4, lines 39-51 ; and column 12, lines 1-16.
(Note that reference is made to U.S. Patent 6,339,552 (which is an English language patent family member of JP 2001-067877) for convenience.)

Also with respect to claims 27, 29, 31, 34, 37, and 40, Taruishi et al disclose that the memory may be utilized in a computer system such as a microcomputer which, as one of ordinary skill in the art would recognize, includes some sort of processor which initiates a predetermined operation with the memory using a clock signal and the various "commands" or instructions discussed throughout Taruishi et al (see column 17, lines 45-47, as well as column 8, lines 16+, e.g.).

With respect to claims 2 and 9, Taruishi et al teaches that the "selectively disabling" comprises selectively disabling sense amplifiers (again see column 6, lines 33-40, e.g.).

With respect to claims 3 and 10, as well as claims 16 and 22, Taruishi et al teach that the "selectively disabling" and "selectively enabling" comprises selectively enabling sense amplifiers as discussed above (again see column 6, lines 33-40). The selective enabling and disabling of the sense amplifiers in Taruishi et al may be considered to occur in response to the beginning and end of a "predetermined" operation such as when a particular bank is selected/deselected for a read or write operation, i.e. the enabling of the sense amplifiers is performed in response to the beginning of a read/write operation when a bank is selected for operation and the disabling of the sense amplifiers is performed in response to the end or completion of a particular predetermined operation such as a read or write operation when a bank is deselected.

With respect to claim 4, Taruishi et al teaches reading a data strobe signal (DQS) which controls reading and writing operations in an SDRAM memory in a

well known manner, and also teaches delaying the data strobe signal. Taruishi et al further teaches that data input and output operations may be synchronized to the edge of a data strobe signal that appears on a memory bus in connection with the predetermined operation or a delayed data strobe signal so as to provide reliable data input and output operations (see column 7, lines 32-59, e.g.).

With respect to claims 5 and 12, Taruishi et al also teach "communicating" signals associated with a double data rate (DDR) synchronous dynamic random access memory (SDRAM) device over the memory bus (see column 1, lines 5-10 and column 5, lines 13-15, e.g.).

With respect to claims 6 and 7, as well as claims 13-14, 17-18, 23-24, 28 and 30, one of ordinary skill in the art would readily appreciate that the operation for which a particular bank may be selected in Taruishi et al may be a read or write operation.

With respect to claim 11, Taruishi et al teach that data input and output and input operations may be synchronized to the edge of a data strobe signal that appears on a memory bus in connection with the predetermined operation (again see column 7, lines 32-59, e.g.).

With respect to claims 19 and 25, the apparatus of Taruishi et al includes circuitry for controlling various compgnents of a memory and thus the "apparatus" of Taruishi et al may be broadly considered to be a memory "controller."

With respect to claims 20 and 26, Taruishi et al teaches that the apparatus may comprise a memory device such as an SDRAM device as discussed above (again see column 1, lines 5-10 and column 5, lines 13-15, e.g.).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 5-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art (see page 1, line 4 to page 2, line 8 of the specification, e.g.) in view of Huang et al.

With respect to claim 1, as well as claims 15, 27, and 31-42, applicants' admitted prior art discloses a method and apparatus for controlling operations in a memory such as a synchronous dynamic random access memory (SDRAM), the method including amplifying data signals from a memory bus using sense amplifiers and "sampling" the amplified data signals (see page 1, line 4 to page 2, line 8 of the specification, e.g.), but does not teach selectively disabling the amplification by the (sense) amplifiers in response to the “absence" of a predetermined operation in order to reduce power consumption.

Huang et al similar discloses a method and apparatus for controlling operations in a memory including amplifying data signals in a memory, and teaches selectively disabling the sense amplifiers in response to the "absence" of a predetermined operation in order to reduce power consumption (see column 1 , lines 46-51*, column 2, lines 39-54*, column 5, line 48 to column 6, line 24, e.g.). Huang et al also specifically teach selectively disabling sense amplifiers in a synchronous dynamic random access memory (SDRAM).

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to selectively disable the sense amplifiers in the SDRAM of applicants' admitted prior art in response to the "absence" of a predetermined operation because Huang et al teaches that a reduced power consumption may be obtained in such an SDRAM, a highly desirable feature in a memory device operating with a high frequency clock signal such as an SDRAM.

With respect to claim 8, as well as claims 21 and 29, and claim 9, Huang et al teach selectively disabling the sense amplifiers in response to the "absence" of a predetermined operation, and thus one of ordinary skill in the art would have found it obvious to enable the sense amplifiers during the "presence" of a predetermined operation on the bus.

Also with respect to claims 27 and 29, applicants' admitted prior ad discloses that SDRAMS may be utilized in computer systems which include a memory controller and, as one of ordinary skill in the art would appreciate, a

processor which initiates a predetermined operation with the memory using a clock signal and various "commands" or instructions.

With respect to claims 2-3 and 6, as well as claims 13, 16-17, 22-23, 28 and 30, Huang et al teach that the "selectively disabling" comprises selectively disabling sense amplifiers, and that the selectively disabling is performed in response to the end or completion of a particular predetermined operation such as a read data output operation (again see column 1, lines 46-51 and column 6, lines 17-24).

With respect to claim 5, as well as claims 12, 20 and 26, applicants' admitted prior art teaches that the apparatus may comprise a memory device such as a double data rate (DDR) SDRAM device (see page 1, lines 10-23 and page 2, lines 5-8 of the present specification).

With respect to claim 7, as well as claims 14, 18 and 24 (and claims 28 and 30), while Huang et al only specifically teaches selectively disabling the sense amplifiers in an SDRAM for a read operation, one of 6rdinary skill in the art at the time the claimed invention was made provided with this teaching would have found it readily obvious to also selectively disable the sense amplifiers in the SDRAM of applicants' admitted prior art for a write operation so as to further decrease or reduce the amount of power consumption in the computer system.

With respect to claim 10, Huang et al teaches selectively disabling the sense amplifiers in response to the “absence" of a predetermined operation, and thus one of ordinary skill in the ad would have found it obvious to enable the

sense amplifiers during the presence of a predetermined operation, as discussed above with respect to claim 8.

Thus, it would have been obvious to enable the sense amplifiers at the beginning, or during the presence, of a predetermined operation, and then to disable the sense amplifiers during the absence, or at the end or completion, of the predetermined operation, in order to maximize power savings.

With respect to claim 11, applicants' admitted prior art discloses that signals are communicated to and from the SDRAM device in synchronization with the edges of a data strobe signal that appears on a memory bus (see page 1, lines 10-13 of the present specification) and thus it would have been obvious to synchronize a sense amplifier enable/disable signal in order to reliably amplify the data signals at the appropriate timing.

With respect to claims 19 and 25, applicants' admitted prior art discloses that the "apparatus" may be a memory controller (see page 1, lines 6-9 and page 2, lines 1-4 of the present specification).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art (see page 1, line 4 to page 2, line 8 of the specification, e.g.) in view of Huang et al as applied to claims 1-3 and 5-30 above (see numbered paragraph 8), and further in view of Yanagawa (US Patent Application Publication#2001/0046163).

With respect to claim 4, applicants' admitted prior art in view of Huang et al disclose a method and apparatus for controlling operations in a memory such

as a synchronous dynamic random access memory (SDRAM) including amplifying data signals from a memory bus using sense amplifiers, "sampling" the amplified data signals, and selectively disabling the amplification by the (sense) amplifiers in response to the "absence" of a predetermined operation in order to reduce power consumption (see numbered paragraph 8 above, e.g.).

Applicants' admitted prior art also teaches that data signals are communicated to and from the SDRAM device in synchronization with the edges of a data strobe signal that appears on a memory bus (see page 1, lines 10-13 of the present specification), but does not teach delaying the data strobe signal and synchronizing communication of the signals to and from the SDRAM device in synchronization with an edge of the delayed data strobe signal.

Yanagawa similarly discloses a SDR/M device in which signals are communicated to and from the SDRAM device in synchronization with the edges of a data strobe signal in a well known manner, and additionally teaches delaying the data strobe signal and synchronizing communication of the signals to and from the SDRAM device in synchronization with an edge of the delayed data strobe signal in order to reliably control the input and output of data from the memory device (see paragraphs (0004) - (0005) and (0010) - (0012), e.g.).

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to delay a data strobe signal and synchronize communication of the signals to and from an SDRAM device in synchronization with an edge of the delayed data strobe signal, as taught by Yanagawa, in the SDRAM device of applicants' admitted prior art in view of

Huang et al as previously discussed, in order to reliably control the input and output of data from the memory device.

Response to Arguments

With respect to applicants' arguments regarding the 35 USC 112 rejection set forth in the previous Office action, examiner agrees, and has, accordingly, removed the rejection.

With respect to applicants' argument that examiner's interpretation of "memory bus" is unreasonable, examiner respectfully disagrees. Applicants' amendment to claim 1, for example, (as well as claims 8, 15, 21, 27, 29, 31, 34, 37, and 40, merely recites the definition of a memory bus. For extrinsic evidence to prove the inherency of the definition, examiner respectfully refers applicant to pages 1 and 2 of the instant specification, which discusses same.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 703.306.5903. The examiner can normally be reached on 9-4-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703.308.1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christian P. Chace